

JK LAKSHMIPAT UNIVERSITY

DIGITAL CIRCUIT AND SYSTEMS  
(EE1120)

Activity 11

Design 8:1 multiplexer structural and dataflow

using VHDL language.

Date : 27th March 2024

Name : Bobby Sharma

Roll no. = 2023BTECH023

# AIM: Design and Simulation of 8 to 1 Multiplexer using Structural Modelling (use 2:1 mux) and data flow modelling both in VHDL language using Xilinx

SOFTWARE REQUIRED: Xilinx ISE tool in your device.

THEORY: A multiplexer is a combinational circuit featuring numerous data inputs and a solitary output, the selection of which depends on control or select inputs. To manage N input lines, log2(N) selection lines are essential, or conversely, for 2^n input lines, n selection lines are requisite. Multiplexers are alternatively termed as "N-to-1 selectors," parallel-to-serial converters, many-to-one circuits, and universal logic circuits. Their primary utility lies in augmenting the quantity of data transmissible over a network within a specified timeframe and bandwidth.

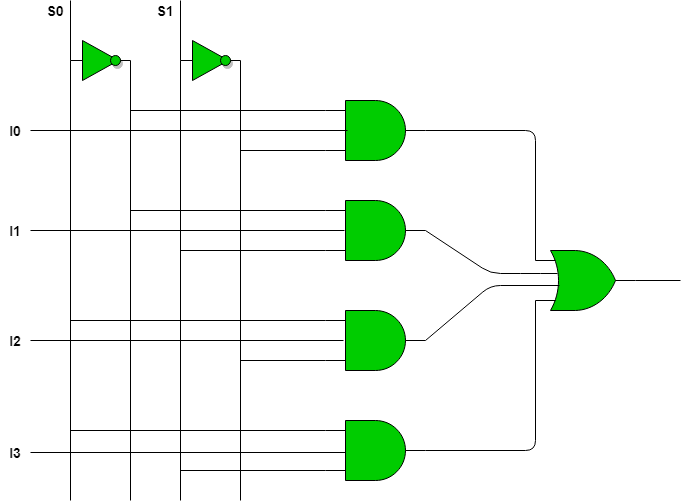


Figure 1

We can make 8:1 multiplexer from 2:1 multiplexer as shown in figure 2:

A diagram of a circuit

Description automatically generated

Figure 2

OBSERVATION: The observed outputs of multiplexer are as follows:

USING DATAFLOW:

VHDL Code: RTL Diagram:

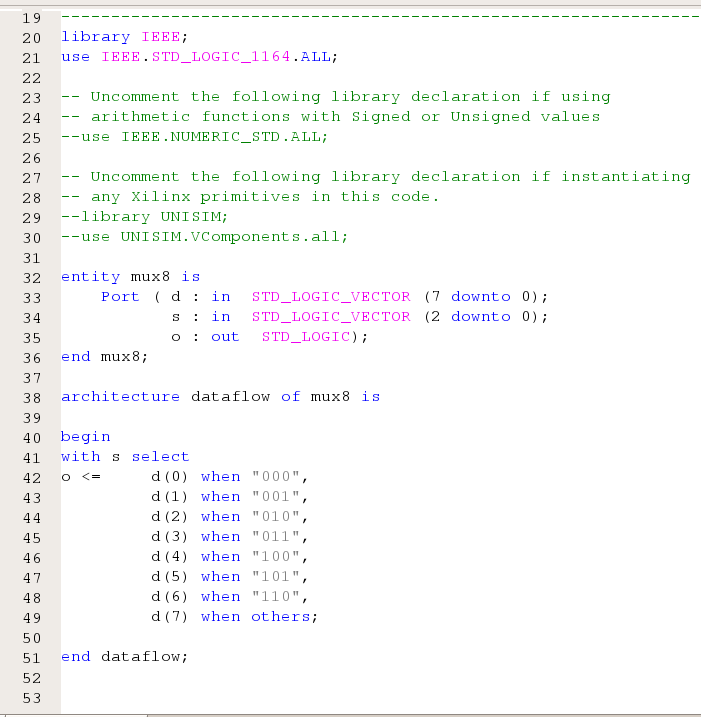
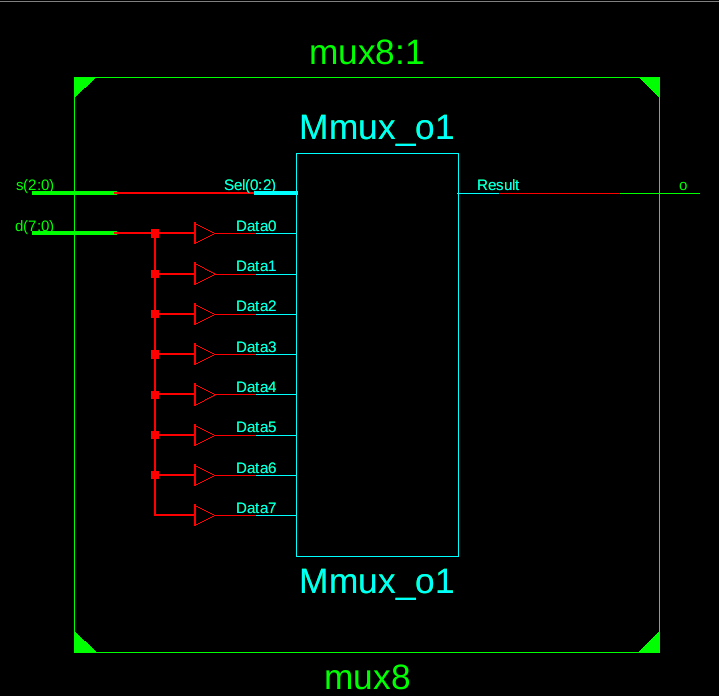
 

Figure 3 Figure 4

Test Bench Code:

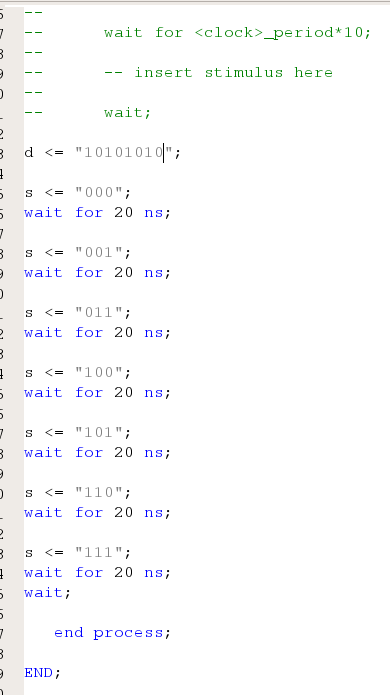


Figure 5

Waveform:

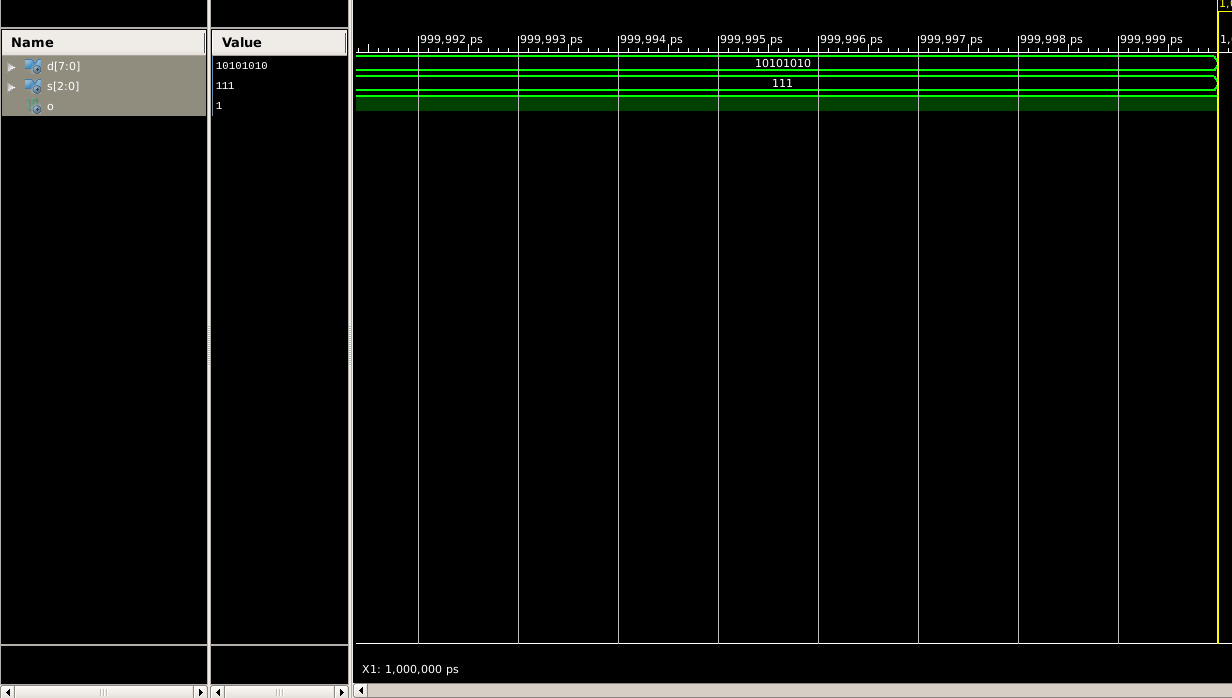


Figure 6

USING STRUCTURAL BY USING 2:1 MULTIPLEXER :

VHDL Code: RTL Diagram:

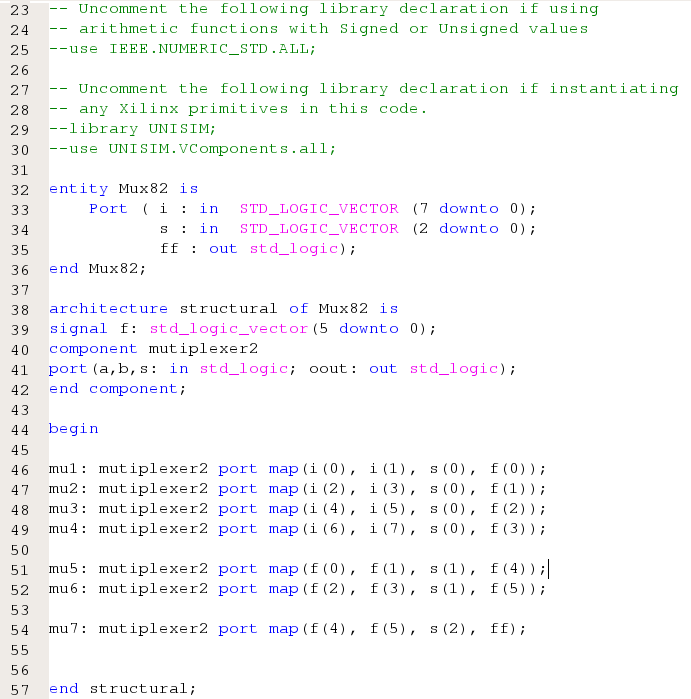
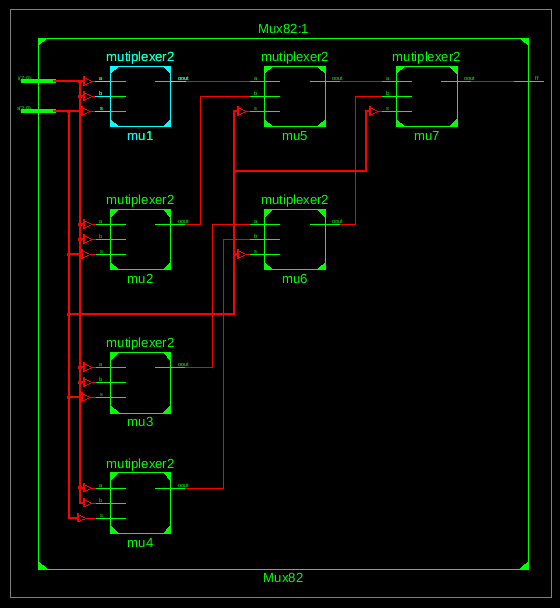
 

Figure 7 Figure 8

Test Bench Code:

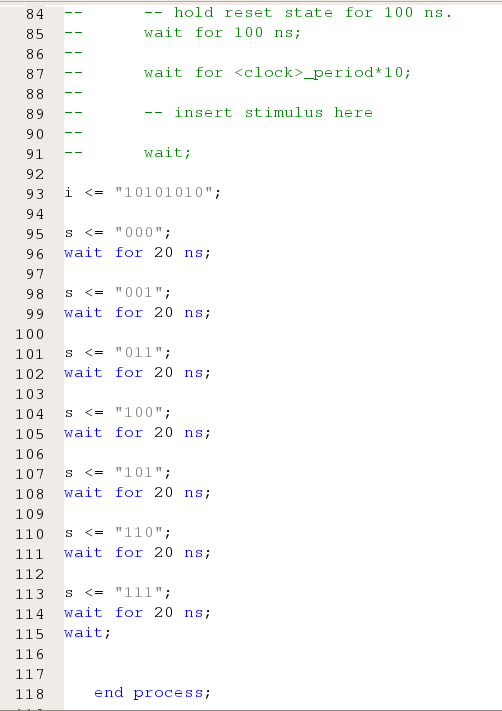


Figure 9

Waveform:

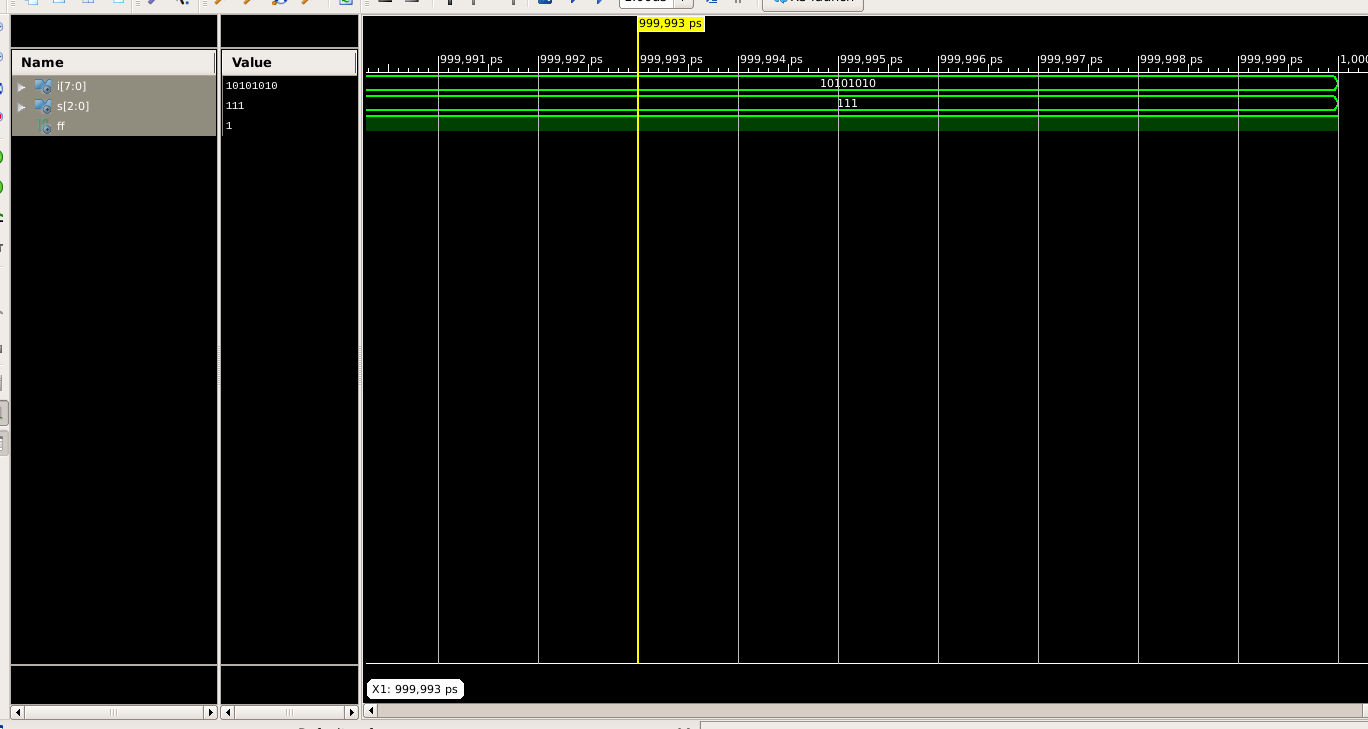


Figure 10

Here the yellow line in figure 6 and 10 represents the input (I(vector) = 10101010 and S(vector) = 111) and therefore the I7 will be represented as the output which in this case is 1. The table for 8:1 multiplexer lists all possible combinations of inputs (S2, S1, and S0) and the corresponding outputs (F).

|  |  |  |  |
| --- | --- | --- | --- |
| S2 | S1 | S0 | F |
| 0 | 0 | 0 | I0 |
| 0 | 0 | 1 | I1 |
| 0 | 1 | 0 | I2 |
| 0 | 1 | 1 | I3 |
| 1 | 0 | 0 | I4 |
| 1 | 0 | 1 | I5 |
| 1 | 1 | 0 | I6 |
| 1 | 1 | 1 | I7 |

Table 1

The Equation can be drawn as :

F = (S2)’(S1)’(S0)’I0 + (S2)’(S1)’(S0)I1 + (S2)’(S1)(S0)’I2 + (S2)’(S1)(S0)I3 + (S2)(S1)’(S0)’I4 + (S2)(S1)’(S0)I5 + (S2)(S1)(S0)’I6 + (S2)(S1)(S0)I7

# RESULT: We have concluded the Equation of 8:1 multiplexer using VHDL language in Xilinx ISE Tool.

APPLICATION IN DAILY LIFE:

* **Data Routing:** In digital systems, data often needs to be routed from various sources to a single destination. An 8:1 multiplexer can be used to select one of eight data sources and pass its output to the destination based on control signals.
* **Memory Addressing:** In computer memory systems, a multiplexer can be used to select a specific memory address. In an 8-bit memory system, an 8:1 multiplexer can be used to choose one of 8 memory locations.
* **Signal Switching:** Multiplexers can be used to switch between different signals in communication systems. For example, in telecommunications, multiple input signals may need to be selectively routed to a single transmission line based on specific conditions or commands.
* **Control Unit Design:** In computer architecture, multiplexers are often used in the design of control units. They can be used to select control signals or data paths based on various conditions or instructions.